

*gmt*  
*1/1*  
a gate insulating layer on the substrate over at least a portion of the surface region of the first sector and the surface region of the second sector; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.

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*Sub*  
*H3*  
*T*  
*2*

6. The transistor of claim 5, wherein the first sector has a narrower line width than a line width of the gate.

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7. (Amended) The transistor of claim 5, in which the gate comprises a first portion over the first sector and a second portion over the second sector; and

the first portion is in a predetermined ratio with respect to the second portion.

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9. The transistor of claim 5, wherein the first sector is separated from the source region and from the drain region by substantially equal distances.